TWO-STAGE MULTIPLIER CIRCUIT

Abstract of the Disclosure

The invention relates to methods and apparatus that receive an integration result, receive logic states of data bits corresponding to the integration result, and perform a high-speed multiplication operation. Embodiments of the invention selectively multiply the integration result according to the logic states of the corresponding data bits. Advantageously, relatively large integration results corresponding to data bit transitions that do not include a change of logic states, such as logic 0 to logic 0 or logic 1 to logic 1, can be multiplied by zero (0). Relatively smaller integration results corresponding to integrations of data bit transitions including a change in logic states, such as from logic 0 to logic 1 or from logic 1 to logic 0, can be multiplied by one (1) and by negative one (-1).